REMARKS

A. Status of the Claims

Claims 1-94 are pending in the application. Claims 6, 33, 34, 59, 60, 83, and 84 were rejected under 35 USC 102(b) as being anticipated by Iwasaki, US Patent No. 6,034,436. Claims 6, 7, 15, 28, 29, 33-35, 43, 59, 69, 83-85, and 86 were rejected under 35 USC 102(b) as being anticipated by Amanuma, US Publication No. 2001/0038115.

Claims 7-14, 27, 35-42, 55, 61-68, 73, and 86-93 were rejected under 35 USC 103(a) as being unpatentable over Iwasaki.

B. 35 USC 102(b) Rejections: Claims 1-6, 30-34, 56-60, 74, 81-84, and 94

Claims 6, 33, 34, 59, 60, 83, and 84 were rejected under 35 USC 102(b) as being anticipated by Iwasaki.

Claim 6 has been amended to recite a structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising: a first plurality of vias, each having a top end and a bottom end; a second plurality of vias, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping; a first routing level at a first height, said first level connected to the first plurality of vias at the bottom end of each first via; and a second routing level at a second height, said second level connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height, wherein both routing levels are formed above a substrate, wherein the first and second vias are evenly spaced and have a common first pitch, and further comprising a third routing level, the third routing level above the first and second vias connected at the top end of each first and second via, vertically opposite the first and second routing levels, wherein the third

routing level comprises memory lines in a memory array, and wherein the first plurality of vias are not connected to any routing level above the first routing level and below the third routing level, and wherein the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level.

The Examiner identifies U1, U2, and U3 of Fig. 7b as the third routing level; S2 as the second routing level, and S1 as the first routing level. Applicants will respectfully maintain, however, that S1 and S2 can not be characterized as routing levels.

A routing level provides electrical connectivity to devices formed at a certain level in an integrated circuit. Interconnects A1, A2, and A3 of Fig. 7b are formed at one routing level, while interconnects U1, U2, and U3 are formed at another. The purpose of through-holes T1, T2, and T3 is to connect interconnects A1, A2, and A3 to interconnects U1, U2, and U3, respectively (col. 5, lines 35-39):

> ... and through-holes T1, T2 and T3 filled with a conductive material, such as tungsten, designated by D1, D2 and D3 **for connecting the third layer interconnects A1, A2 and A3 with overlying fourth layer interconnects U1, U2, and U3** formed on top of the through-holes. [emphasis added]

It appears, then, that interconnects A1, A2, and A3 are members of one routing level, and further that interconnects U1, U2, and U3 are members of a different routing level. Interconnects A1, A2 and A3 (as well as A4 through A9, described in later embodiments) are described as "functional interconnects" (col. 7 line 27) and "ordinary" interconnects (col. 5, line 46), in both cases to distinguish them from layers S1 and S2 which apparently have an entirely different function:

> The first and second layer underlying interconnects S1, S2 and S2 **are formed solely in order for underlying the through-holes T2, T1 and T3** during the step of forming functional interconnects of first conductive layer and second conductive layer, and hence, not connected to any of interconnects except for the through-holes. [emphasis added]

As Iwasaki describes, the *only* purpose of S1 and S2 is to underlie the through-holes T1, T2, and T3 during their formation. This function is described further at col. 5, lines 61-64:

> During an etching step to form the through-holes T1, T2 and T3, the underlying interconnects S1, S2 and S2 **have a function for prevention of penetration by the through-holes** toward the bottom of the device.

S1 and S2 apparently serve as etch stop layers, and are intended to prevent overetch of the through-holes T1, T2, and T3. This is further made apparent in that Iwasaki describes the advantage of increased contact area between interconnects A1, A2, and A3 and the conductive material D1, D2, and D3 of through-holes T1, T2, and T3 (see col. 6, lines 43-50). Iwasaki makes no mention of the contact area to S1 and S2, as this contact is apparently of no importance, since S1 and S2 are not functional or ordinary interconnects, but merely etch stop layers.

Summarizing, S1 and S2 are clearly formed solely to serve as etch stop layers. There is no teaching in Iwasaki that S1 and S2 are routing levels; in fact interconnects A1-A9 (shown in the embodiments of Figs. 7b through 10b) are referred to repeatedly as "functional" interconnects *in contrast to* S1 and S2.

If, however, the Examiner does not accept Applicants' contention that S1 and S2 cannot be considered routing levels, then Applicants will respectfully point out that, as amended, claim 6 also recites that the first plurality of vias are not connected to any routing level above the first routing level and below the third routing level, and wherein the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level. Yet in the embodiments of Iwasaki, through-holes T1, T2, and T3 are connected to interconnects A1, A2, and A3, which form

a routing level between interconnects U1, U2, and U3 and etch stops S1 and S2. Claim 6 recites that there is no intervening routing level, and thus distinguishes even if S1 and S2 are considered to be routing levels.

Independent claims 33, 59, and 83 are amended in this response, and thus they and their dependent claims distinguish over Iwasaki by a similar rationale. Applicants respectfully request reconsideration.

C. 35 USC 102(b) Rejections: Claims 6, 7, 15, 28, 29, 33-35, 43, 59, 69, 83-85, and 86

Claims 6, 7, 15, 28, 29, 33-35, 43, 59, 69, 83-85, and 86 were rejected under 35 USC 102(b) as being anticipated by Amanuma.

Claim 6 has been amended to recite a structure for providing multilevel electrical connectivity within an integrated circuit, the structure comprising: a first plurality of vias, each having a top end and a bottom end; a second plurality of vias, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping; a first routing level at a first height, said first level connected to the first plurality of vias at the bottom end of each first via; and a second routing level at a second height, said second level connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height, wherein both routing levels are formed above a substrate, wherein the first and second vias are evenly spaced and have a common first pitch, and further comprising a third routing level, the third routing level above the first and second vias connected at the top end of each first and second via, vertically opposite the first and second routing levels, wherein the third routing level comprises memory lines in a memory array, and ***wherein the first plurality of vias are not connected to any routing level above the first routing level and below the***

third routing level, and wherein the second plurality of vias are not connected to any routing level above the second routing level and below the third routing level.

The Examiner finds, in Fig. 2 of Amanuma, a second plurality of vias, each having a top end and a bottom end, where "the second vias are considered to extend from the bottom of structure 30 to the top of structure 7". In Fig. 2 of Amanuma, however, these second vias are connected to a routing level 10 above the second routing level and below the third routing level. Thus independent claims 6, 33, 59, and 83, and their dependent claims, distinguish over the embodiment pictured in Fig. 2 of Amanuma.

Applicants respectfully request reconsideration.

D. 35 USC 103(a) Rejections: Claims Claims 7-14, 27, 35-42, 55, 61-68, 73, and 86-93

Claims 7-14, 27, 35-42, 55, 61-68, 73, and 86-93 were rejected under 35 USC 103(a) as being unpatentable over Iwasaki.

Claims 7-14 depend from claim 6, which distinguishes over the references for the reasons described in Section B of these remarks. Similarly, claims 35-42 depend from claim 33, which distinguishes over the references for the reasons described in Section B of these remarks. Claims 61-68 depend from claim 59, which distinguishes over the references for the reasons described in Section B of these remarks. Similarly, claims 86-93 depend from claim 83, which distinguishes over the references for the reasons described in Section B of these remarks.

In addition, claim 14 adds the limitation that the memory array is a monolithic three dimensional memory array. The Examiner finds that Iwasaki does not explicitly teach use of staggered vias of the claim in a monolithic three dimensional memory array:

> ... it is considered nonetheless obvious to one of ordinary skill in the art to employ the improved through-hole structure of Iwasaki to any known memory device structure or array.

Applicants will respectfully assert, however, that the simple fact that a structure, such as the interconnect structure of Fig. 7b of Iwasaki, is known, does not make its use desirable, or obvious, in every memory array. If this were the case, this interconnect structure would be widely used in memory arrays, but, as the Examiner will be aware, it is not. Many reasons, including complexity of interconnect fabrication and layout constraints, will lead those skilled in the art to choose other interconnect methods.

A monolithic three dimensional memory array, having multiple stacked device levels formed above a substrate, has very specific layout requirements. Several such memory arrays have been described, as in Johnson et al., US Patent No. 6,034,882; in Zhang, US Patent No. 5,835,396; in Cleeves, US Patent No. 6,664,639; and in Scheuerlein et al., US Publication No. 2004/0125629. None of these monolithic three dimensional memory arrays uses or suggests the use of the through-holes of Iwasaki, despite having the motivation suggested by the Examiner, "to reduce the occupied area for the interconnections." Absent some suggestion that such interconnects are particularly advantageous in this context, Applicants maintain a *prima facie* case of obviousness has not been made.

The same rationale applies to the rejection of claims 27, 42, 55, 68, 73, and 90.

In addition, claims 55 and 73 have also been amended to include the limitation that the vias make no connection to an intervening routing level between the first and third routing levels, as were claims 6, 33, 59, and 83, and thus additionally distinguish for the reasons explained in section B of these remarks.

Applicants respectfully request reconsideration.

CONCLUSION

In view of the preceding Remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicants **respectfully request an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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